

REMARKS

Claims 1-8 and 10-24 are pending in this application. Claim 9 is canceled and claim 24 is added herein. Claims 1, 10, and 18 have been amended herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

Claims 1 and 6-8 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,159,826 to Kim, *et al.*

The remainder of the claims were rejected under 35 U.S.C. 103(a) as being obvious over Kim, *et al.* in view of one or more additional prior art sources.

The applicant strongly disagrees with the Examiner that the phrase "on the chip scribe lines" in the Kim, *et al.* reference is sufficient to anticipate or even render obvious any of the independent claims that clearly require the bond areas and probe areas of the bond pad to be "on the semiconductor chip". As anyone skilled in the art will appreciate chip 'scribe lines' are not on the semiconductor chip itself and are cut away during separation or singulation of the chip from the wafer structures. That is, they are "outside -not on- the semiconductor chip itself. However, in an effort to move the prosecution of this case forward, the three independent claims have been amended one each in three different ways to include a limitation that unquestionably patentably distinguishes these claims from the Kim, *et al.* reference.

For example, claim 1 now requires a bond wire connection to coexist on the chip with the probe area as shown in FIG. 7 of the application.

This condition is in no way even suggested, much less taught by the Kim, *et al.* reference. Furthermore, this conduction would never reasonably occur with the Kim, *et al.* structure since the probe area of Kim, *et al.* will be cut away well before bond wires are attached to the chip.

Independent claim 10, on the other hand, requires that the probe areas and bond areas of the bond pad be located inside a perimeter defined by separating scribe lines, and that the area inside the perimeter not include scribe lines.

Finally, independent claim 18 requires that the probe area be present on the semiconductor chip even after being separated from the wafer.

Therefore, it is respectfully submitted that independent claims 1, 10, and 18 do now patentably define over all references of record and are allowable. Likewise, all of the dependent claims are also allowable for depending from an allowable claim as well as for these own limitations.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,

19 August 2005  
Date

James C. Kesterson  
James C. Kesterson  
Attorney for Applicant  
Reg. No. 25,882

Slater & Matsil, L.L.P.  
17950 Preston Rd., Suite 1000  
Dallas, Texas 75252-5793  
Tel. 972-732-1001  
Fax: 972-732-9218